

WHAT IS CLAIMED IS:

1. A method of verifying the adequacy of test patterns, comprising the steps of

forming test patterns which are to be applied to a device under test in order to conduct a testing of the device under test and expected values used for determining whether device output data which is delivered from the device under test in response to one of the test pattern is acceptable or faulty, both in the cycle basis format;

converting the test pattern into an event basis format data;

storing the test pattern in the event basis format in a first memory;

reading device output data in the event basis format which is obtained as a result of execution of a logic simulation with respect to the device under test from a dump file storage and storing it in a second memory;

deriving device output data stored in the second memory which corresponds to the test pattern stored in the first memory;

converting the derived device output data into the cycle basis format data;

and determining whether or not all of the logical states in the converted device output data are compared against corresponding expected values.

2. A method according to Claim 1, further comprising the step of comparing the converted device output data against the expected value and if a non-coincidence is found in the result of comparison, rendering a determination that the test pattern which corresponds to this device output data is faulty.

3. A method according to Claim 2 in which the step of determining whether or not the comparison against the expected value has been made

comprises the step of determining whether or not a timing for the comparison against the expected value has occurred during a time interval from a change in the logic state of the device output data to a next change in the logic state.

4. A method according to Claim 3 in which the determination of whether or not the timing for the comparison has occurred comprises setting a flag to one state for each change in the logic state of the converted device output data, setting the flag to the other state in response to the occurrence of the timing for the comparison, examining whether the flag is in its one state or the other state immediately before each change in the logic state of the converted device output data, and determining the absence of the timing for the comparison if the flag is in its one state.

5. A method according to Claim 3 further comprising the step of in the absence of the timing for the comparison, storing a test cycle number of the test pattern in which the timing for the comparison has not occurred in a storage.

6. A method according to Claim 2 in which two of the first memories and the two of the second memories are provided and wherein while the device output data corresponding to the test pattern which is stored in one of the first memories is derived from one of the second memories, a test pattern and device output data are stored in the other of the first memories and in the other of second memories, respectively, thus allowing the two first and second memories to operate in an interleaved manner between deriving corresponding device output data and storing of the test pattern and the device output data.

7. An apparatus for rapidly verifying the adequacy of test patterns, comprising
an LSI tester simulator for forming test patterns which are to be

applied to a device under test in order to conduct a testing of the device and expected values used for determining whether device output data which is delivered from the device under test in response to one of the test patterns is acceptable or faulty, both in the cycle basis format;

a cycle/event basis converter for converting a test pattern delivered from the LSI test simulator into data in the event basis format;

a first memory for storing the test pattern in the event basis format which is delivered from the cycle/event basis converter;

a dump file storage for storing device output data of the device under test which is obtained as a result of execution of a logic simulation with respect to the device under test in the event basis format;

a second memory for storing device output data which is read from the dump file storage;

a comparing and synchronizing unit for extracting the device output data which corresponds to the test pattern stored in the first memory, and for delivering the extracted data to the LSI tester simulator as device output data;

and determination timing default detecting means for detecting whether or not the determining timing for comparison of the device output data against expected values which takes place in the LSI tester simulator has existed for each change in the state of the device output data.

8. An apparatus according to Claim 7 in which the determination timing default detecting means comprises logic storage means which is reset to one logic state in response to the determination timing for comparison and inverted to the other logic state in response to a change in the logic state of the device output data, and error detecting means which detects an error by detecting the other state which is already stored in the logic storage means before a change in the logic state of the device output data causes the logic

state in the logic storage means to be inverted to the other logic state.

9. An apparatus according to Claim 7, further comprising a report formulator for storing a test cycle number in which the default of the determination timing has occurred each time the determination timing default detecting means detects the default of the determination timing.